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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,875	02/27/2002	Carl Mizyuabu	1376.0200080	4740

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EXAMINER	
PATEL, NITIN C	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,875	MIZYUABU ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-43 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21,28,29,31-35,37,38 and 40-43 is/are rejected.

7)☒ Claim(s) 22-27,30,36 and 39 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 February 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 18 November 2002.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 43 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 5, 38, and 40, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Paver, US Patent 6,049,882.

4. As to claims 1, and 38, Paver discloses an apparatus and method comprising the steps of:

a. identifying [by counting number of instructions waiting in queue] an operating characteristic [delay (cycle time)] based on a number of commands queued [instruction queue length] in an instruction buffer [instruction buffer/FIFO/register inherent to instruction pipe-line processing], and

b. adjusting a system characteristic [system performance] based on the operating characteristic [delay (cycle time)], wherein power consumption is modified [adjusted] based on the system characteristic [system performance][col. 5, lines 60 – 67, col. 6, lines 1 – 14, fig. 8].

5. As to claim 2, Paver discloses that the steps are performed through set of discrete components [fig. 5, 8].

6. As to claim 3, Paver discloses the number of commands [instruction] queued [an instruction queue length] including number of instructions to be processed by a processor [500] associated with the system [col. 6, lines 1- 4, fig. 5, 8].

7. As to claim claims 4, 7, and 40, Paver discloses an instruction processing with processor [fig. 5, 8], which inherently teaches to process different types of instruction including display instructions by processor associated with the system [it is inherent property processor to process different types of instructions].

8. As to claim 5, Paver discloses the operating characteristic [delay (cycle time)] includes a number of pending operation [number of instructions waiting in a queue to be processed] [col. 6, lines 1 – 8].

9. Claims 1 – 10, 21, 38, 40 – 41, and 43, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yu et al. [hereinafter as Yu], US Patent 6,463,542 B1.

10. As to claims 1, and 38, Yu discloses a system and method comprising the steps of:

a. identifying [by checking] an operating characteristic [network activity] based on a number of commands queued [SRAM buffer empty indicator] in an instruction buffer [SRAM buffer], and

b. adjusting [by power management] a system characteristic [normal/power-down mode] based on the operating characteristic [network activity], wherein power consumption is modified based on the system characteristic [normal/power-down mode][col. 1, lines 39 – 67, col. 2, lines 1 – 5, col. 4, lines 19 – 67, col. 5, lines 1 – 58, fig. 2].

11. As to claim 2, Yu discloses that the steps are performed through set of discrete components [fig. 2].

12. As to claim 3, Yu discloses a computer system for data communication with CPU [66], system memory [62] including transmit SRAM buffer [18 b], receive SRAM buffer [18 a],

MAC, with interfaces [MMU, BIU] which inherently teaches to process instructions by processor associated with the system [it is inherent property of CPU to process instructions].

13. As to claims 4, 7, and 40, Yu discloses a computer system for data communication with CPU [66], system memory [62] including transmit SRAM buffer [18 b], receive SRAM buffer [18 a], MAC, with interfaces [MMU, BIU] which inherently teaches to process different types of instruction including display instructions, power management command by processor associated with the system [it is inherent property of CPU to process different types of instructions][col. 5, lines 1 – 17].

14. As to claim 5, Yu teaches the operating characteristic [network I/F is active/idle] includes a number of pending operation [SRAM buffer empty indicator indicating no pending operation] [col. 4, lines 19 – 67, col. 5, lines 1 – 58, fig. 2].

15. As to claim 6, Yu discloses a computer system for data communication with network I/F is active/idle [the operating characteristic] with network activity, therefore he teaches including fill rate [receive rate] associated with the instruction buffer [receive SRAM buffer 18 a][fig. 2].

16. As to claims 8 – 10, and 41, Yu discloses a computer system for data communication with network I/F in a packet switched Ethernet network [IEEE 802.3] [col. 2, lines 33 – 36], which inherently teaches number of bits used to represent multimedia data including video and audio data too.

17. As to claim 21, Yu teaches the operating characteristic [network activity] is based upon buffer fullness [buffer empty that means network is idle].

18. As to claims 43, Yu discloses a system characteristic [normal/power-down mode] with power management to support power.

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

20. Claims 28 – 29, 31 – 35, and 37 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Veltchev et al. [hereinafter as Valtchev], US Patent 6,590,730 B2.

21. As to claim 28, Veltchev discloses a system comprising:

a. an instruction buffer [18, buffer] to store pending instructions [to store block to be played];

b. a buffer monitor [is inherent to buffer management/monitoring][col. 4, lines 7 – 8] to: track a buffer statistic [amount of the block left to be played];

c. provide a buffer status [by providing a trigger] of said buffer statistic to a power threshold [when buffer data remaining to be played reaches a low threshold level];

d. a power module [inherent to power management] to initiate a power conservation feature [HDD transition from the IDLE mode to SLEEP mode] based on said buffer status [block is loaded into buffer][col. 2, lines 23 – 67, col. 3, lines 1 – 26, fig. 1].

22. As to claim 29, Veltchev discloses a buffer management system with monitoring buffer data remaining to be played [pending instructions] with low threshold level [col. 1, lines 60 64, col. 2, lines 59 – 67, col. 3, lines 1 – 6], which inherently teaches a storage device to store a low level threshold.

23. As to claims 31 – 33, and 37, Veltchev discloses a system [10] including a HDD [12], interface [14], CPU [16], a buffer [18], system memory [20] where CPU executes program code including playing the digital musical data [col. 3, lines 1 – 2], which inherently includes multimedia, display, and audio instructions too.

24. As to claims 34 – 35, Veltchev discloses a buffer management system with monitoring buffer data remaining to be played [pending instructions] with low threshold level [col. 1, lines 60 64, col. 2, lines 59 – 67, col. 3, lines 1 – 6] and the block is loaded into buffer, triggering HDD transition from IDLE to SLEEP mode [buffer fullness].

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 11 – 20, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. [hereinafter as Yu], US Patent 6,463,542 B1 as applied to claims 1 – 10, 21, 38, 40 – 41, and 43, above, and further in view of Gupta et al. [hereinafter as Gupta], Us Patent 5,996,083.

27. As to claims 11, and 42, Yu discloses a method comprising the steps of: identifying [by checking] an operating characteristic [network activity] based on a number of commands queued [SRAM buffer empty indicator] in an instruction buffer [SRAM buffer], and adjusting [by power management] a system characteristic [normal/power-down mode] based on the operating characteristic [network activity], wherein power consumption is modified based on the system

characteristic [normal/power-down mode][col. 1, lines 39 – 67, col. 2, lines 1 – 5, col. 4, lines 19 – 67, col. 5, lines 1 – 58, fig. 2].

However, Yu does not teach explicitly power management reducing clock speed based on indications that SRAM buffers are empty and no receive or transmit activity is detected. In summary, he does not teach to manage power consumption by changing the clock speed.

Gupta discloses a microprocessor system and method to shut down or adjust the execution rate [clock speed] of function unit [col. 5, lines 49 –57] with clock dividers that divides the master clock signal down by integer ratios (e.g. 1/2, 1/3, ¼...1/16) responsive to a corresponding values in power control register fields [col. 3, lines 48 – 67, col. 4, lines 1 – 35, col. 6, lines 40 –65].

It would have been obvious to one of ordinary skill in art, having the teachings of Yu and Gupta before him at the time of invention was made, to modify the power management indication mechanism for supporting power saving mode in computer system disclosed by Yu to include an improved power management as taught by Gupta in order to obtain microprocessor controlling the power consumption of individual function units and power control register fields set by software which has much greater ability to look out into future requirement of functional units and software control permits power management capabilities not possible with hardware and software possesses knowledge that is unavailable to hardware make more informed power management decisions that have the least impact on performance [col. 3, lines 40 – 67, col. 4, lines 1 – 67].

28. As to claims 12, and 16 – 17, Gupta teaches the use of transistor interposed between function unit and a supply terminal to alter a nominal power provided to match an amount of power needed for the speed used [col. 7, lines 57 – 57 – 67].

29. As to claims 13, and 18, Gupta discloses different functional units including multimedia unit [col. 5, lines 40 – 57] and teaches selectively switching between a 32 bit and 64 bit external interface to reduce power of I/O [col. 4, lines 21 – 24].

30. As to claims 14 – 15, and 19 – 20, Gupta discloses different functional units including multimedia unit, therefore he teaches multimedia data including video and audio data [col. 5, lines 40 – 57].

31. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

32. Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Allowable Subject Matter

33. Claims 22 – 27, 30, 36, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 7:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
January 27, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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